In re Patent Application of
DE SANTIS ET AL.
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In the Claims:

Claims 1-6 (Cancelled).

7. (New) A sensing circuit for a memory cell and comprising:

a first bias current generator connected between a first voltage reference and a first inner circuit node;

at least one second reference current generator connected to the first voltage reference;

a comparator having a first input terminal connected to a comparison circuit node that is connected to said at least one second reference current generator, a second input terminal connected to a circuit node that is connected to the first inner circuit node, and at least one output terminal forming at least one output terminal of the sensing circuit;

a cascode-configured bias circuit connected between the inner circuit node and a matching circuit node, said cascode-configured bias circuit also connected to a second voltage reference; and

a current/voltage conversion stage connected to the matching circuit node, to the comparison circuit node, and to a third voltage reference.

8. (New) A sensing circuit according to Claim 7, wherein the first voltage reference is a supply voltage, and a third voltage reference is ground.

9. (New) A sensing circuit according to Claim 7, wherein said cascode-configured bias circuit comprises:

a first transistor connected between the inner circuit node and the matching circuit node, said first

transistor comprising a control terminal; and

an operational amplifier having an output terminal connected to the control terminal of said first transistor, a first input terminal connected to the second voltage reference and a second input terminal connected to the output terminal.

10. (New) A sensing circuit according to Claim 9, wherein said first transistor comprises a P-channel MOS transistor.

11. (New) A sensing circuit according to Claim 7, wherein said current/voltage conversion stage comprises:

a second transistor that is diode-configured and is connected between the matching circuit node and the third voltage reference, said second transistor comprising a control terminal; and

a third transistor connected between the comparison circuit node and the third voltage reference, said third transistor comprising a control terminal connected to the control terminal of said second transistor.

12. (New) A sensing circuit according to Claim 11, wherein said second transistor and said third transistor comprise N-channel MOS transistors.

13. (New) A sensing circuit according to Claim 7, wherein said at least one second reference current generator comprises a plurality of reference current generators forming a plurality of branches connected to a plurality of inputs of said comparator; and wherein said at least one output terminal

of said comparator comprises a plurality of output terminals for forming a plurality of output terminals of the sensing circuit.

14. (New) A memory comprising:

at least one memory cell; and

at least one sensing circuit connected to said at least one memory cell and comprising

a first bias current generator connected to a first voltage reference,

at least one second reference current generator connected to the first voltage reference,

a comparator having a first input terminal connected to a comparison circuit node that is connected to said at least one second reference current generator, a second input terminal connected to a circuit node that is connected to said first bias current generator, and at least one output terminal forming at least one output terminal of the sensing circuit,

a bias circuit connected to said first bias current generator, and

a current/voltage conversion stage connected to said bias circuit, to the comparison circuit node, and to a second voltage reference.

15. (New) A memory according to Claim 14, wherein the first voltage reference is a supply voltage, and the second voltage reference is ground.

16. (New) A memory according to Claim 14, wherein

said bias circuit comprises:

a first transistor connected between said first bias current generator and said current/voltage conversion stage, said first transistor comprising a control terminal; and

an operational amplifier having an output terminal connected to the control terminal of said first transistor, a first input terminal connected to a third voltage reference and a second input terminal connected to the output terminal.

17. (New) A memory according to Claim 16, wherein said first transistor comprises a P-channel MOS transistor.

18. (New) A memory according to Claim 14, wherein said current/voltage conversion stage comprises:

a second transistor that is diode-configured and is connected between said bias circuit and the second voltage reference, said second transistor comprising a control terminal; and

a third transistor connected between the comparison circuit node and the second voltage reference, said third transistor comprising a control terminal connected to the control terminal of said second transistor.

19. (New) A memory according to Claim 18, wherein said second transistor and said third transistor comprise N-channel MOS transistors.

20. (New) A memory according to Claim 14, wherein said at least one second reference current generator comprises a plurality of reference current generators forming a

plurality of branches connected to a plurality of inputs of said comparator; and wherein said at least one output terminal of said comparator comprises a plurality of output terminals for forming a plurality of output terminals of said sensing circuit.

21. (New) A method for forming a sensing circuit for a memory cell, the method comprising:

connecting a first bias current generator between a first voltage reference and a first inner circuit node;

connecting at least one second reference current generator to the first reference voltage;

connecting a comparator having a first input terminal to a comparison circuit node that is connected to the at least one second reference current generator, a second input terminal connected to a circuit node that is connected to the first inner circuit node, and at least one output terminal forming at least one output terminal of the sensing circuit;

connecting a bias circuit between the inner circuit node and a matching circuit node, the bias circuit also being connected to a second voltage reference; and

connecting a current/voltage conversion stage to the matching circuit node, to the comparison circuit node, and to a third voltage reference.

22. (New) A method according to Claim 21, wherein the first voltage reference is a supply voltage, and the third voltage reference is ground.

23. (New) A method according to Claim 21, wherein

the bias circuit comprises:

a first transistor connected between the inner circuit node and the matching circuit node, the first transistor comprising a control terminal; and

an operational amplifier having an output terminal connected to a control terminal of the first transistor, a first input terminal connected to the third voltage reference and a second input terminal connected to the output terminal.

24. (New) A method according to Claim 23, wherein the first transistor comprises a P-channel MOS transistor.

25. (New) A method according to Claim 21, wherein the current/voltage conversion stage comprises:

a second transistor that is diode-configured and is connected between the matching circuit node and the third voltage reference, the second transistor comprising a control terminal; and

a third transistor connected between the comparison circuit node and the third voltage reference, the third transistor comprising a control terminal connected to the control terminal of the second transistor.

26. (New) A method according to Claim 25, wherein the second transistor and the third transistor comprise N-channel MOS transistors.

27. (New) A method according to Claim 21, wherein the at least one second reference current generator comprises a plurality of reference current generators forming a

plurality of branches connected to a plurality of inputs of the comparator; and wherein the at least one output terminal of the comparator comprises a plurality of output terminals for forming a plurality of output terminals of the sensing circuit.